REMARKS

This paper is filed in reply to the non-final Office Action of June 16, 2003. The Applicants first amend the specification to correct a U.S. patent number cited in the specification, as described below. The Applicants then respond to the Restriction Requirement set forth in the Office Action.

Amendment to the Specification

The Applicants have amended the U.S. patent number shown on page 1, line 22 of the specification from "5,456,189" to --5,465,189--. Essentially, the "5" and the "6" were transposed in the specification as originally filed due to a typographical error. This typographical error is further shown comparing the subject matter of the originally cited patent number and the corrected patent number. U.S. Patent No. 5,456,189 is titled "Shipping Pallet" while U.S. Patent No, 5,465,189 is titled "Low Voltage Triggering Semiconductor Controlled Rectifiers." Therefore, the Applicants submit that the amendment to the specification does not add any new matter to the application and may be properly entered.

Restriction Requirement

In the Office Action of June 16m 2003, the Examiner asserts that the application presents two patentably distinct species of the claimed invention: Embodiment 1 described in Figs. 2A - C and Embodiment 2 described in Fig. 3. Alternatively, the Examiner asserts that the application sets forth four patentably distinct species of the claimed invention: Claims 1-3 and 7-11 described in Figs. 2A-C; Claims 4-6 described in Fig. 3; Claims 12 and 14-18 described in Figs. 2A-C; and Claim 13 described in Fig. 3.

The Applicants request that the Examiner reconsider the requirement for restriction as discussed below. However, as required under 37 C.F.R. 1.143, the Applicant provisionally elect the claims directed to Embodiment 1 as identified by the Examiner. The Applicants further submit that Claims 1-3, 7-11, 12, and 14-18 are directed to Embodiment 1. Therefore, the Applicants provisionally elect Claims 1-3, 7-11, 12, and 14-18.

The Examiner is respectfully reminded that, as set forth in MPEP 816:

> 'The particular reasons relied on by the examiner for holding that the inventions as claimed are either independent or distinct should be concisely stated. A mere statement of conclusion is inadequate. The reasons upon which the conclusion is based should be given.

The Applicants submit that the Examiner has merely concluded that the inventions as claimed are independent or distinct and has not provided the requisite reasons for that conclusion. Therefore, the Applicants submit that the restriction requirement set forth in the Office Action of June 16, 2993 is improper. As such, reconsideration is respectfully requested and the Examiner is respectfully requested to withdraw the restriction requirement.

However, if the Examiner does not withdraw the restriction requirement, the Applicants respectfully request continue the examination of the application with elected Claims 1-3, 7-11, 12, and 14-18. The Applicants further note that non-elected Claims 4 - 6 and 13 depend either directly or indirectly upon elected claims. Therefore, non-elected Claims 4-6 and 13 should be found to be allowable if the claims from which they depend are found to be allowable.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being facsimile transmitted to FAX No.: 703-872-9318 and addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

July 7, 2003
(Date of Deposit)

Ross A. Schmitt
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7-7-2003
(Date)

Encl.: Appendix A - 2 pages

Respectfully submitted,

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TITLE

ESD PROTECTION CIRCUIT TRIGGERED BY LOW VOLTAGE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a electrostatic discharge (ESD) protection circuit triggered by low voltage. Particularly, the present invention relates to an ESD protection circuit comprising a durable metal oxide semiconductor (MOS).

Description of the Related Art

ESD is a major concern for estimating the reliability of an integrated circuit (IC). All components of the IC having external connections, such as input pins, output pins, I/O pins, and power-bus pins must have the capability to discharge ESD stress and protect the core circuit of the IC.

Referring to Fig.1, the conventional ESD protection circuit in US patent no. 6,465,189 discloses a lateral semiconductor control rectifier (LSCR) and a MOS transistor to achieve ESD protection. As shown in Fig.1, the ESD protection circuit comprises a p-substrate 16, an N-well 18, a p-type doped region 20 in the N-well 18 as an anode, and an NMOS 22. The NMOS 22 comprises a gate 26, an n-type second doped region 30 and an n-type first doped region 28. The anode 20, the N-well 18, the P-substrate 16 and the second doped region 30 form the LSCR. The first doped region 28 is formed at the junction between the N-well 18 and the P-substrate 16 to dissipate the current in the N-well 18. A p+ first contact region 34 and an n+ second contact region 36 are respectively formed in the P-substrate 16 and the N-well 18 as shown in Fig.1. The second contact

region 36 and the anode 20 are both coupled to a pad 12, then coupled to a core circuit. The gate 26 of the MOS 22 and the first contact region 34 are coupled to a power pad, such as Vss.

When ESD stress occurs at the pad 12, the major voltage drop occurs at the junction between the N-well 18 and the P-substrate 16. Due to the difference of doped concentration between the N-well 18 and the P-substrate 16, an avalanche breakdown voltage is lowest at the junction thereof to allow the current to dissipate into the substrate 16, triggering the LSCR. The ESD stress is discharged through the LSCR and thus the core circuit is protected.

The resistance of the source and drain of the MOS have reduced with the development of the self-aligned-silicide (Salicide) process. A large voltage drop occurs between the first doped region 28 and the gate 26 because of the smaller resistance of the first doped region 28. The gate oxide under the gate 26 is designed to tolerate only low voltages (about 3V) under normal conditions, not the high voltage stress resulting here. A conventional solution is to have the salicide process performed at the core circuit, but not at the ESD protection circuit. By doing so, a photo mask, creating extra manufacturing costs, is needed.

Another solution is to increase the resistance of the first doped region 28 by increasing the length of the first doped region 28. Unfortunately, additional increases in manufacturing costs also result from the increased area of the first doped region 28. Worst of all, the resistance between the first doped region 28 and the MOS is not evenly distributed, causing uneven loading on the MOS gate which then damages the gate oxide of the gate 26.

SUMMARY OF THE INVENTION